AW-NM512

IEEE 802.11 b/g/n Wireless LAN

And Bluetooth Module

Datasheet

Rev. C

DF

(For Standard)

FORM NO.: FR2-015_ A Responsible Department：WBU Expiry Date: Forever

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Features

Overview

- Integrates Infineon solutions of CYW43439_A1 WiFi /BT/SoC
- SDIO v2.0 interfaces support for WLAN
- High speed UART and PCM for Bluetooth
- Lead-free Design
- 12.0mm(L) x 12.0mm(W) x 1.5 mm(H) 47 pin LGA package
- With Crystal(XTAL)

WiFi

- Single band 2.4 GHz 802.11 b/g/n
- SDIO v2.0, including DS and HS modes
- Security–WEP, WPA/WPA2/WPA3, AES (HW), TKIP (HW), CKIP (SW), WMM/WMM-PS/WMM-SA
- Data Rate up to 72.2Mbps

Bluetooth

- Supports extended Synchronous Connections (eSCO), for enhanced voice quality by allowing for retransmission of dropped packets
- Adaptive Frequency Hopping (AFH) for reducing radio frequency interference
- Maximum UART baud rates up to 4 Mbps
- Supports Bluetooth 5.0's LE Secure Connections
- Fully supports Bluetooth Core Specification version 5.0 + (Enhanced Data Rate) EDR features:
  - Adaptive Frequency Hopping (AFH)
  - Quality of Service (QoS)
  - Extended Synchronous Connections (eSCO) — Voice Connections
  - Fast Connect (interlaced page and inquiry scans)
  - Secure Simple Pairing (SSP)
  - Sniff Subrating (SSR)
  - Encryption Pause Resume (EPR)
  - Extended Inquiry Response (EIR)
  - Link Supervision Timeout (LST)
- Interface support – Host Controller Interface (HCI) using a high-speed UART interface and PCM for audio data

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Revision History

Document NO: **R2-2512-DST-01**

Version	Revision Date	DCN NO.	Description	Initials	Approved
A	2020/09/23	DCN018490	● First Initial	QM.TAN	N.C Chen
B	2021/01/20	DCN020585	● Update Specifications Table	QM.TAN	N.C Chen
C	2021/04/13	DCN021226	● Cypress to Infineon ● Update BLE Specification	QM.TAN	N.C Chen

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1. Introduction

1.1 Product Overview

AzureWave Technologies, Inc. introduces the advanced IEEE 802.11 b/g/n WLAN and Bluetooth combo module - AW-NM512. The module is targeted to mobile and embedded devices which need small footprint package, low power consumption, and multiple OS support. The module supports 2.4GHz IEEE 802.11n MAC/baseband/radio, and Bluetooth 5.0 compliance. It also features an integrated Power Management Unit (PMU), Power Amplifiers (PAs), and a Low Noise Amplifier (LNA) to address the needs of mobile devices that require minimal power consumption and compact size. By using AW-NM512, the customers can easily enable the Wi-Fi and BT embedded applications with the benefits of high design flexibility, short development cycle, and quick time-to-market. Specified in the IEEE 802.11 standard minimize the system power requirements by using AW-NM512. In addition to the support of WPA/WPA2/WPA3 and WEP encryption, the AW-NM512 also supports the IEEE 802.11i security standard through AES and TKIP acceleration hardware for faster data encryption. For the video, voice and multimedia applications the AW-NM512 support 802.11e Quality of Service (QoS). The host interface is SDIO v2.0 interface.

For Bluetooth operation, the AW-NM512 is Bluetooth 5.0 compliant. The Bluetooth transmitter also features a Class 1 power amplifier. The AW-NM512 supports extended Synchronous Connections (eSCO), for enhanced voice quality by allowing for retransmission of dropped packets, and Adaptive Frequency Hopping (AFH) for reducing radio frequency interference. It also incorporates all Bluetooth 5.0 features including Secure Simple Pairing, Sniff Subrating, and Encryption Pause and Resume. An independent, high-speed UART is provided for the Bluetooth host interface. The Bluetooth subsystem presents a standard Host Controller Interface (HCI) via a high speed UART and PCM for audio.

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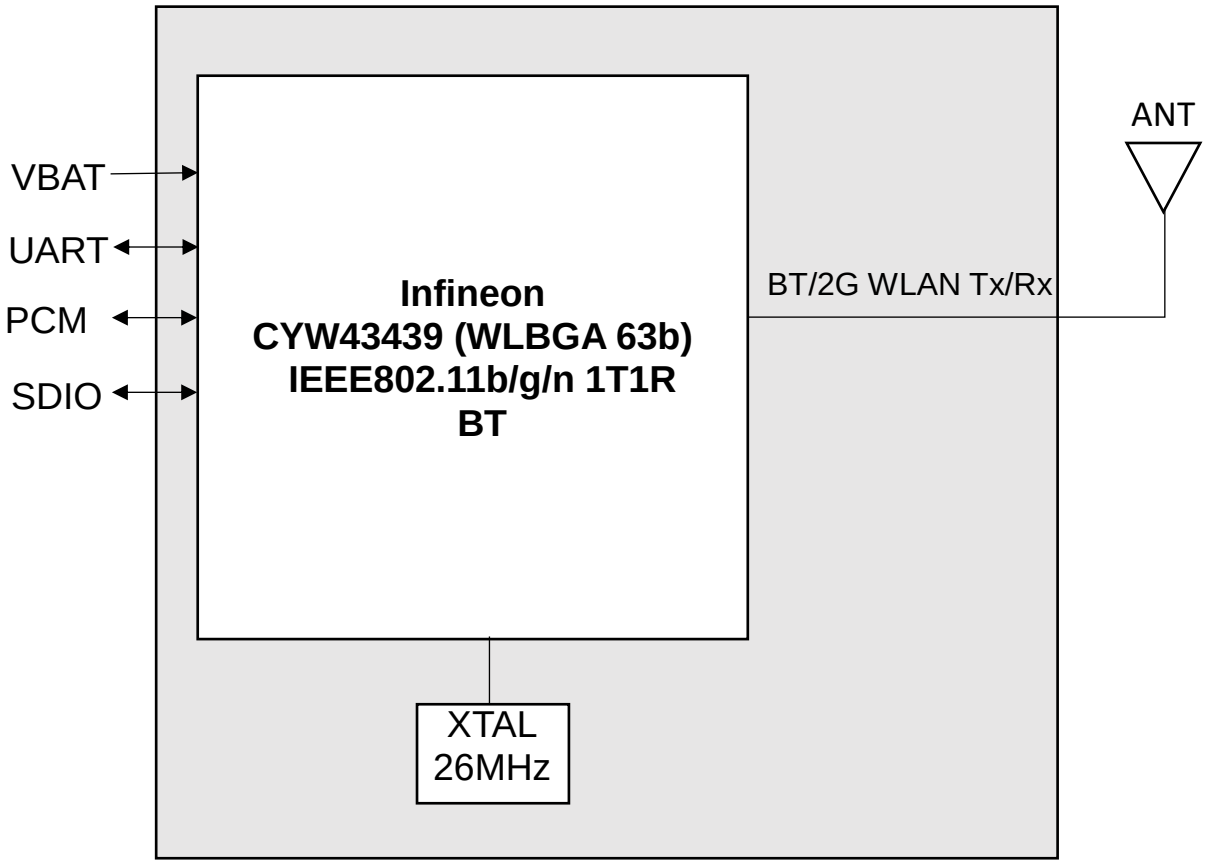
1.2 Block Diagram



AW-NM512 Block Diagram

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1.3 Specifications Table

1.3.1 General

Features	Description
Product Description	IEEE 802.11 b/g/n Wireless LAN and Bluetooth Module
Major Chipset	Infineon CYW43439 (WLBGA 63b)
Host Interface	WiFi + BT ● SDIO + UART
Dimension	12.0mm(L) x 12.0mm(W) x 1.5 mm(H)
Form factor	● LGA module, 47 pins
Antenna	For LGA, “1T1R, external” ANT1(Main)：WiFi/Bluetooth → TX/RX
Weight	0.4g

1.3.2 WLAN

Features	Description
WLAN Standard	IEEE 802.11 b/g/n, 1T1R
WLAN VID/PID	N/A
WLAN SVID/SPID	N/A
Frequency Range	2.4 GHz ISM Bands 2.412-2.472 GHz
Modulation	DSSS, OFDM, BPSK(9/6Mbps), QPSK(18/12Mbps), DBPSK(1Mbps), DQPSK(2Mbps), CCK(11/5.5Mbps), 16-QAM(36/24Mbps), 64-QAM (72.2/54/48Mbps)
Number of Channels	802.11b: USA, Canada and Taiwan – 1 ~ 11 Most European Countries – 1 ~ 13 802.11g: USA and Canada – 1 ~ 11 Most European Countries – 1 ~ 13 802.11n: USA and Canada – 1 ~ 11 Most European Countries – 1 ~ 13

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<table>
<tr><td>Output Power
(Board Level Limit)*</td><td>2.4G
<table>
<tr><td></td><td>Min</td><td>Typ</td><td>Max</td><td>Unit</td></tr>
<tr><td>11b (11Mbps)
@EVM<35%</td><td>16</td><td>18</td><td>20</td><td>dBm</td></tr>
<tr><td>11g (54Mbps)
@EVM≦-25 dB</td><td>14</td><td>16</td><td>18</td><td>dBm</td></tr>
<tr><td>11n (HT20 MCS7)
@EVM≦-27 dB</td><td>13</td><td>15</td><td>17</td><td>dBm</td></tr>
</table></td></tr>
<tr><td>Receiver Sensitivity</td><td>2.4G
<table>
<tr><td></td><td>Min</td><td>Typ</td><td>Max</td><td>Unit</td></tr>
<tr><td>11b (11Mbps)</td><td></td><td>-89</td><td>-84</td><td>dBm</td></tr>
<tr><td>11g (54Mbps)</td><td></td><td>-76</td><td>-71</td><td>dBm</td></tr>
<tr><td>11n (HT20 MCS7)</td><td></td><td>-73</td><td>-68</td><td>dBm</td></tr>
</table></td></tr>
<tr><td>Data Rate</td><td>802.11b: 1, 2, 5.5, 11Mbps
802.11g: 6, 9, 12, 18, 24, 36, 48, 54Mbps
802.11n:MCS 0~7 HT20</td></tr>
<tr><td>Security</td><td>◆ WPA™- WPA2™- and WPA3™ support for powerful encryption and authentication
◆ AES in WLAN hardware for faster data encryption and IEEE802.11i compatibility
◆ Reference WLAN subsystem provides Wi‐Fi Protected Setup (WPS).
Wi-Fi Protected Setup (WPS)</td></tr>
</table>

* If you have any certification questions about output power please contact FAE directly.

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1.3.3 Bluetooth

<table>
<tr><th>Features</th><th>Description</th></tr>
<tr><td>Bluetooth Standard</td><td>Bluetooth 5.0</td></tr>
<tr><td>Bluetooth VID/PID</td><td>N/A</td></tr>
<tr><td>Frequency Range</td><td>2400~2483.5MHz</td></tr>
<tr><td>Modulation</td><td>GFSK (1Mbps), Π/4DQPSK (2Mbps) and 8DPSK (3Mbps)</td></tr>
<tr><td>Output Power</td><td>6≤ Output Power ≤ +10 dBm (Conductive)
<table>
<tr><td></td><td>Min</td><td>Typ</td><td>Max</td><td>Unit</td></tr>
<tr><td>BDR</td><td>6</td><td>8</td><td>10</td><td>dBm</td></tr>
<tr><td>EDR</td><td>6</td><td>8</td><td>10</td><td>dBm</td></tr>
<tr><td>Low Energy</td><td>6</td><td>8</td><td>10</td><td>dBm</td></tr>
</table></td></tr>
<tr><td>Receiver Sensitivity</td><td>
<table>
<tr><td></td><td>Min</td><td>Typ</td><td>Max</td><td>Unit</td></tr>
<tr><td>DH5</td><td></td><td>-91</td><td>-86</td><td>dBm</td></tr>
<tr><td>2DH5</td><td></td><td>-91</td><td>-86</td><td>dBm</td></tr>
<tr><td>3DH5</td><td></td><td>-83</td><td>-79</td><td>dBm</td></tr>
<tr><td>Low Energy</td><td></td><td>-91</td><td>-86</td><td>dBm</td></tr>
</table></td></tr>
</table>

1.3.4 Operating Conditions

Features	Description
Operating Conditions	
Voltage	VBAT:3.2V~4.8V (3.6V Typical)
Operating Temperature	-30℃ to 70 ℃ (Optimal RF performance guarantee -20℃~70 ℃)
Operating Humidity	less than 85% R.H.
Storage Temperature	-40℃ to 85 ℃
Storage Humidity	less than 60% R.H.
ESD Protection	
Human Body Model	1000V
Changed Device Model	300V

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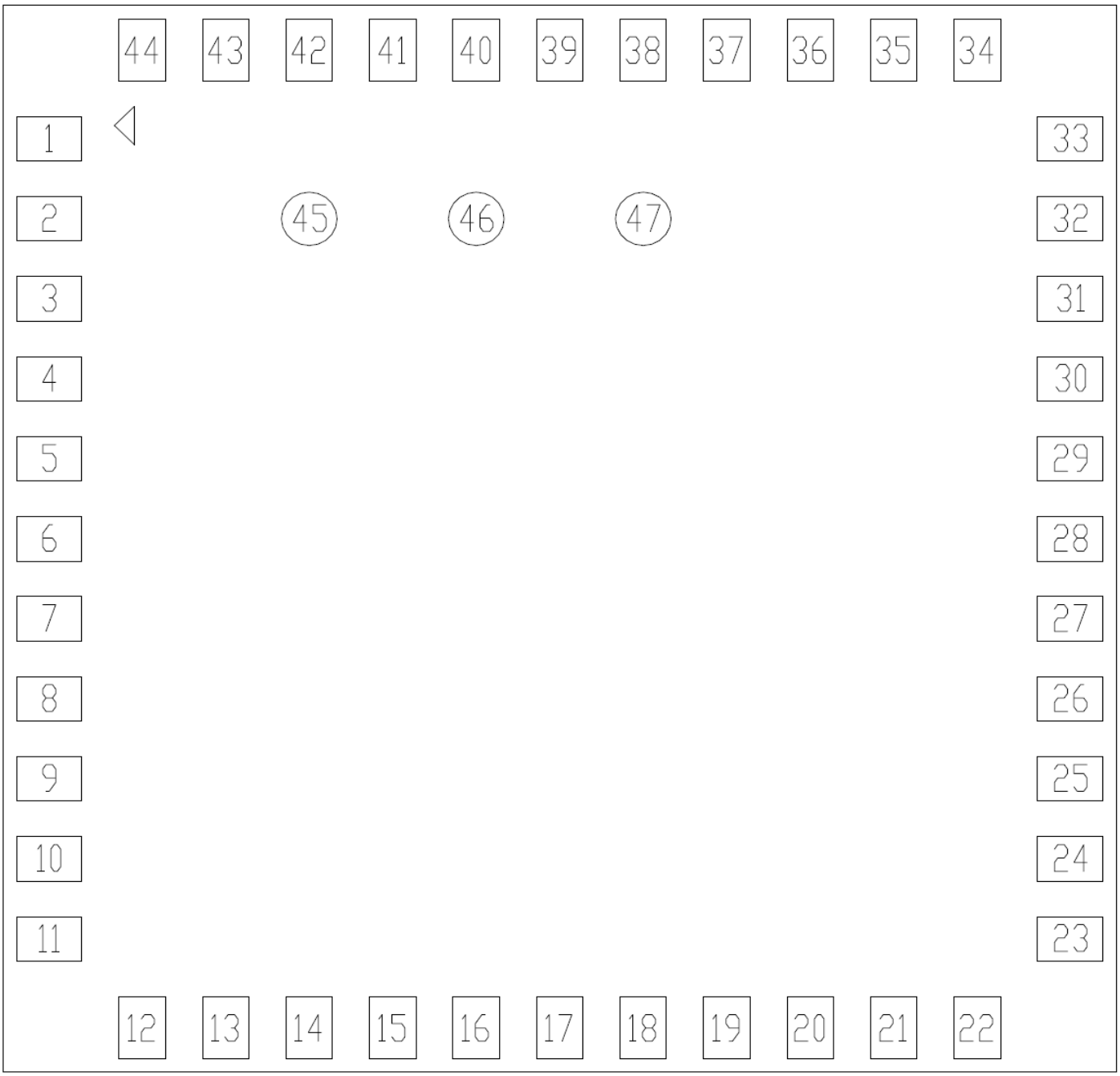
2. Pin Definition

2.1 Pin Map



AW-NM512 Pin Map (Top View)

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2.2 Pin Table

Pin No	Definition	Basic Description	Voltage	Type
1	GND	Ground.		GND
2	WL_BT_ANT	WLAN/BT RF TX/RX path.		RF
3	GND	Ground.		GND
4	NC	Floating Pin, No connect to anything.		Floating
5	NC	Floating Pin, No connect to anything.		Floating
6	BT_WAKE_DEV	HOST wake-up Bluetooth device	VDDIO	I
7	BT_HOST_WAKE	Bluetooth device to wake-up HOST	VDDIO	O
8	CLK_REQ	The module asserts CLK_REQ when Bluetooth or WLAN directs the host to turn on the reference clock. The CLK_REQ polarity is active-high	VDDIO	O
9	VBAT	3.3V power pin	VBAT	PWR
10	NC	Floating Pin, No connect to anything.		Floating
11	NC	Floating Pin, No connect to anything.		Floating
12	WL_REG_ON	Used by PMU to power up or power down the internal regulators used by the WLAN section. Also, when deasserted, this pin holds the WLAN section in reset. This pin has an internal 200k ohm pull down resistor that is enabled by default. It can be disabled through programming.	VDDIO	I
13	WL_HOST_WAKE	WLAN device to wake-up HOST	VDDIO	O
14	SDIO_DATA_2	SDIO Data Line 2	VDDIO	I/O
15	SDIO_DATA_3	SDIO Data Line 3	VDDIO	I/O
16	SDIO_CMD	SDIO Command Input	VDDIO	I/O
17	SDIO_CLK	SDIO Clock Input	VDDIO	I
18	SDIO_DATA_0	SDIO Data Line 0	VDDIO	I/O
19	SDIO_DATA_1	SDIO Data Line 1	VDDIO	I/O
20	GND	Ground.		GND
21	VIN_LDO_OUT	Internal Buck 1.2V voltage generation pin	1.4V	O
22	VDDIO	1.8V-3.3V VDDIO supply for WLAN and BT	VDDIO	PWR
23	VIN_LDO	Internal Buck 1.2V voltage generation pin	1.4V	I
24	LPO	External 32K or RTC clock	0.2~3.3V	I

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25	PCM_OUT	PCM data Out	VDDIO	O
26	PCM_CLK	PCM Clock	VDDIO	I/O
27	PCM_IN	PCM data Input	VDDIO	I
28	PCM_SYNC	PCM Synchronization control	VDDIO	O
29	NC	Floating Pin, No connect to anything.		Floating
30	NC	Floating Pin, No connect to anything.		Floating
31	GND	Ground.		GND
32	NC	Floating Pin, No connect to anything.		Floating
33	GND	Ground.		GND
34	BT_REG_ON	Used by PMU to power up or power down the internal regulators used by the Bluetooth section. Also, when deasserted, this pin holds the Bluetooth section in reset. This pin has an internal 200k ohm pull down resistor that is enabled by default. It can be disabled through programming.	VDDIO	I
35	NC	Floating Pin, No connect to anything.		Floating
36	GND	Ground.		GND
37	NC	Floating Pin, No connect to anything.		Floating
38	NC	Floating Pin, No connect to anything.		Floating
39	GPIO2	Wi-Fi Co-existence pin with LTE(WLAN_SECI_RX)	VDDIO	I
40	GPIO1	Wi-Fi Co-existence pin with LTE(WLAN_SECI_TX)	VDDIO	O
41	UART_RTS_N	High-Speed UART RTS	VDDIO	O
42	UART_OUT	High-Speed UART Data Out	VDDIO	O
43	UART_IN	High-Speed UART Data In	VDDIO	I
44	UART_CTS_N	High-Speed UART CTS	VDDIO	I
45	NC	Floating Pin, No connect to anything.		Floating
46	NC	Floating Pin, No connect to anything.		Floating
47	NC	Floating Pin, No connect to anything.		Floating

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3. Electrical Characteristics

3.1 Absolute Maximum Ratings

Symbol	Parameter	Minimum	Typical	Maximum	Unit
VBAT	Power supply for Internal Regulators	-0.5		6	V
VDDIO	DC supply voltage for digital I/O	-0.5		3.9	V

3.2 Recommended Operating Conditions

Symbol	Parameter	Minimum	Typical	Maximum	Unit
VBAT	Power supply for Internal Regulators	3*	3.6	4.8*	V

***Optimal RF performance is guaranteed only for 3.2V<VBAT<4.8V**

3.3 Digital IO Pin DC Characteristics

Symbol	Parameter	Minimum	Typical	Maximum	Unit
For SDIO Interface VDDIO =1.8V					
VIH	Input high voltage	1.27	-	-	V
VIL	Input low voltage	-	-	0.58	V
VOH	Output High Voltage @ 2mA	1.4	-	-	V
VOL	Output Low Voltage @ 2mA	-	-	0.45	V
For SDIO Interface VDDIO =3.3V					
VIH	Input high voltage	0.625 x VDDIO	-	-	V
VIL	Input low voltage	-	-	0.25 x VDDIO	V
VOH	Output High Voltage @ 2mA	0.75 x VDDIO	-	-	V
VOL	Output Low Voltage @ 2mA	-	-	0.125 x VDDIO	V
Other Digital Interface VDDIO=1.8V					
VIH	Input high voltage	0.65 x VDDIO	-	-	V
VIL	Input low voltage	-	-	0.35 x VDDIO	V
VOH	Output High Voltage @ 2mA	VDDIO – 0.45	-	-	V

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VOL	Output Low Voltage @ 2mA	-	-	0.45	V
Other Digital Interface VDDIO=3.3V					
VIH	Input high voltage	2.00	-	-	V
VIL	Input low voltage	-	-	0.80	V
VOH	Output High Voltage @ 2mA	VDDIO – 0.4	-	-	V
VOL	Output Low Voltage @ 2mA	-	-	0.40	V

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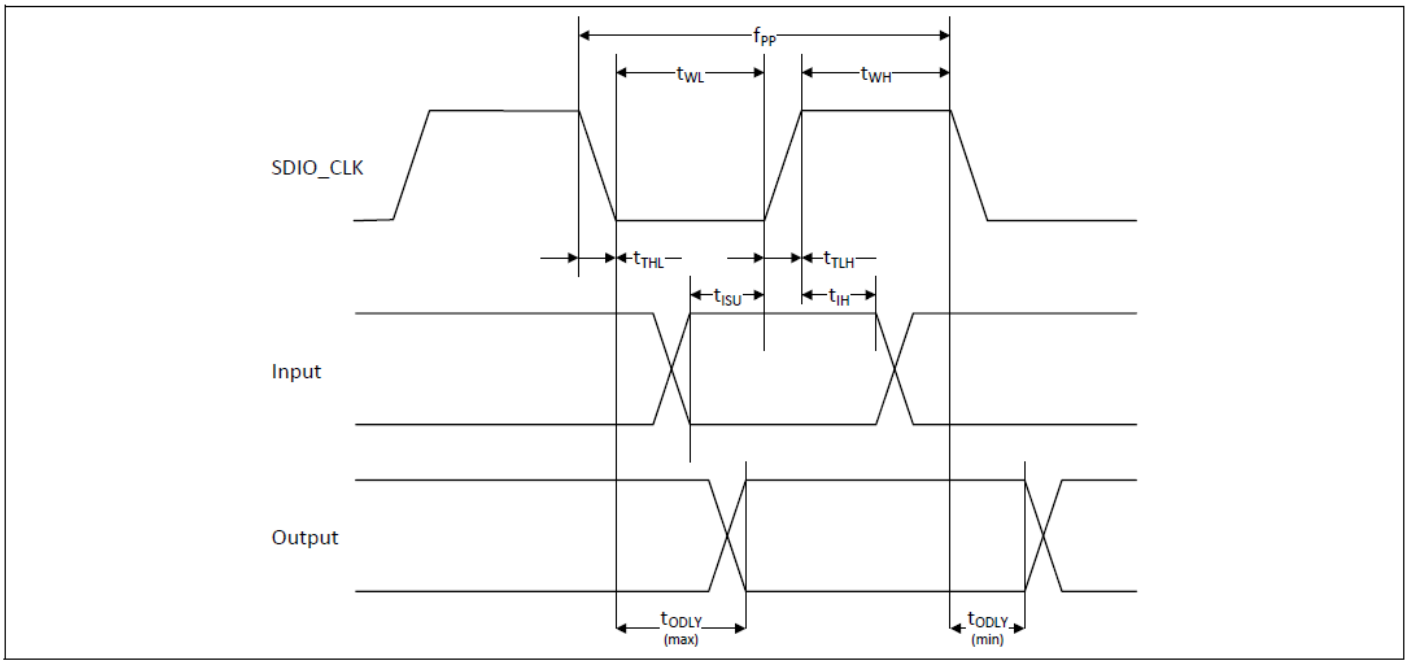
3.4 Host Interface

3.4.1 SDIO



SDIO Bus Timing (Default Mode)

Parameter	Symbol	Minimum	Typical	Maximum	Unit
SDIO CLK (All values are referred to minimum VIH and maximum VIL*)					
Frequency – Data Transfer mode	fPP	0	–	25	MHz
Frequency – Identification mode	fOD	0	–	400	kHz
Clock low time	tWL	10	–	–	ns
Clock high time	tWH	10	–	–	ns
Clock rise time	tTLH	–	–	10	ns
Clock low time	tTHL	–	–	10	ns
Inputs: CMD, DAT (referenced to CLK)					
Input setup time	tISU	5	–	–	ns
Input hold time	tIH	5	–	–	ns
Outputs: CMD, DAT (referenced to CLK)					

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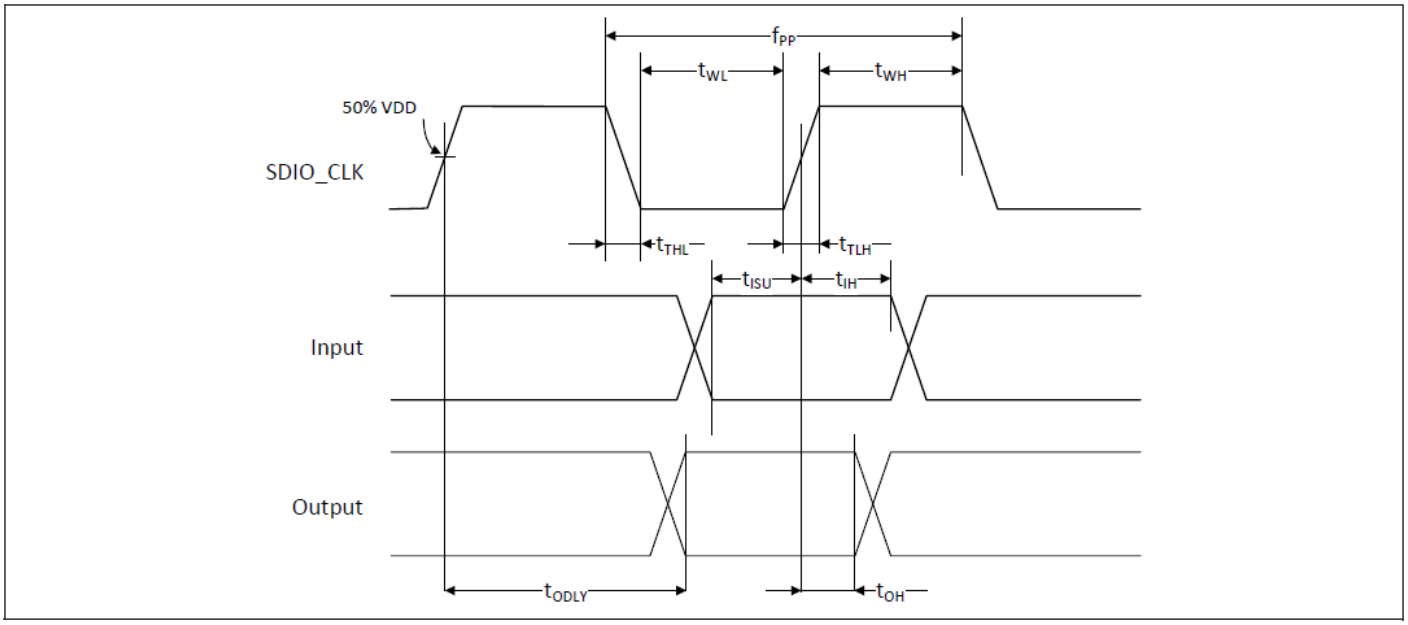
Output delay time – Data Transfer mode	tODLY	0	–	14	ns
Output delay time – Identification mode	tODLY	0	–	50	ns

SDIO Bus Timing Parameters (Default Mode)

* min(VIH) = 0.7 × VDDIO and max(VIL) = 0.2 × VDDIO



SDIO Bus Timing (High-Speed Mode)

Parameter	Symbol	Minimum	Typical	Maximum	Unit
SDIO CLK (all values are referred to minimum VIH and maximum VIL*)					
Frequency – Data Transfer Mode	fPP	0	–	50	MHz
Frequency – Identification Mode	fOD	0	–	400	kHz
Clock low time	tWL	7	–	–	ns
Clock high time	tWH	7	–	–	ns
Clock rise time	tTLH	–	–	3	ns
Clock low time	tTHL	–	–	3	ns
Inputs: CMD, DAT (referenced to CLK)					
Input setup Time	tISU	6	–	–	ns
Input hold Time	tIH	2	–	–	ns

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Outputs: CMD, DAT (referenced to CLK)					
Output delay time – Data Transfer Mode	tODLY	–	–	14	ns
Output hold time	tOH	2.5	–	–	ns
Total system capacitance (each line)	CL	–	–	40	pF

SDIO Bus Timing a Parameters (High-Speed Mode)

* min(Vih) = 0.7 × VDDIO and max(Vil) = 0.2 × VDDIO

3.4.2 UART Interface

The AW-NM512 includes a single UART for Bluetooth. The UART is a standard 4-wire interface (RX, TX, RTS, and CTS) with adjustable baud rates from 9600 bps to 4.0 Mbps. The interface features an automatic baud rate detection capability that returns a baud rate selection. Alternatively, the baud rate may be selected through a vendor-specific UART HCI command.

UART has a 1040-byte receive FIFO and a 1040-byte transmit FIFO to support EDR. Access to the FIFOs is conducted through the AHB interface through either DMA or the CPU. The UART supports the Bluetooth 5.0 UART HCI specification: H4, a custom Extended H4, and H5. The default baud rate is 115.2 Kbaud.

The UART supports the 3-wire H5 UART transport, as described in the Bluetooth specification (“Three-wire UART Transport Layer”).Compared to H4, the H5 UART transport reduces the number of signal lines required by eliminating the CTS and RTS signals.

The AW-NM512 UART can perform XON/XOFF flow control and includes hardware support for the Serial Line Input Protocol (SLIP). It can also perform wake-on activity. For example, activity on the RX or CTS inputs can wake the chip from a sleep state.

Normally, the UART baud rate is set by a configuration record downloaded after device reset, or by automatic baud rate detection, and the host does not need to adjust the baud rate. Support for changing the baud rate during normal HCI UART operation is included through a vendor-specific command that allows the host to adjust the contents of the baud rate registers. The AW-NM512 UARTs operate correctly with the host UART as long as the combined baud rate error of the two

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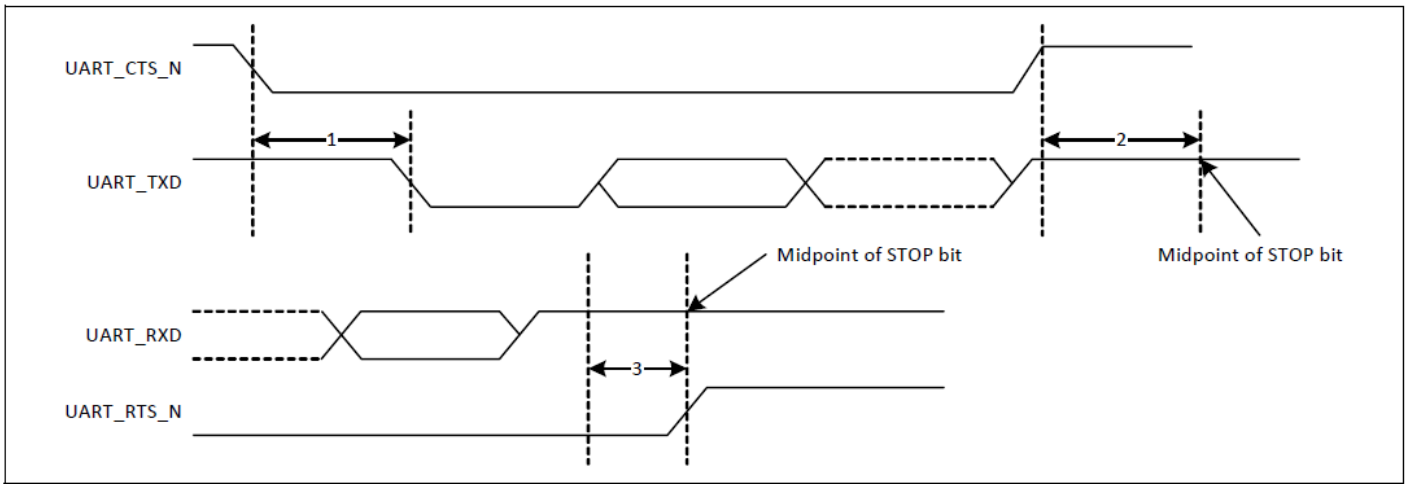
devices is within ±2%.

UART Interface Signals

PIN No.	Name	Description	Type
40	UART_TXD	Bluetooth UART Serial Output. Serial data output for the HCI UART Interface	O
41	UART_RXD	Bluetooth UART Series Input. Serial data input for the HCI UART Interface	I
43	UART_RTS_N	Bluetooth UART Request-to-Send. Active-low request-to-send signal for the HCI UART interface	O
42	UART_CTS_N	Bluetooth UART Clear-to-Send. Active-low clear-to-send signal for the HCI UART interface.	I



UART Timing

	Reference Characteristics	Minimum	Typical	Maximum	Unit
1	Delay time, UART_CTS_N low to UART_TXD valid	–	–	1.5	Bit periods
2	Setup time, UART_CTS_N high before midpoint of stop bit	–	–	0.5	Bit periods
3	Delay time, midpoint of stop bit to UART_RTS_N high	–	–	0.5	Bit periods

UART Timing Specifications

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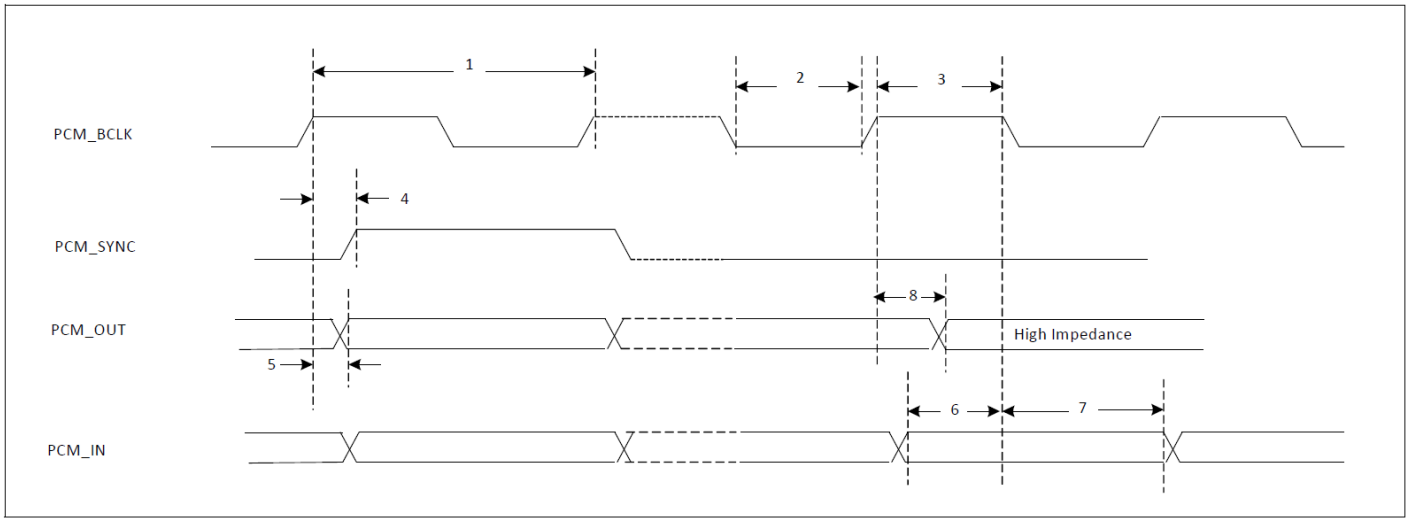
3.4.3 PCM Interface Timing



PCM Timing Diagram(Short Frame Sync, Master Mode)

	Reference Characteristics	Minimum	Typical	Maximum	Unit
1	PCM bit clock frequency			12	MHz
2	PCM bit clock low	41			ns
3	PCM bit clock high	41			ns
4	PCM_SYNC delay	0		25	ns
5	PCM_OUT delay	0		25	ns
6	PCM_IN setup	8			ns
7	PCM_IN hold	8			ns
8	Delay from rising edge of PCM_BCLK during last bit period to PCM_OUT becoming high impedance	0		25	ns

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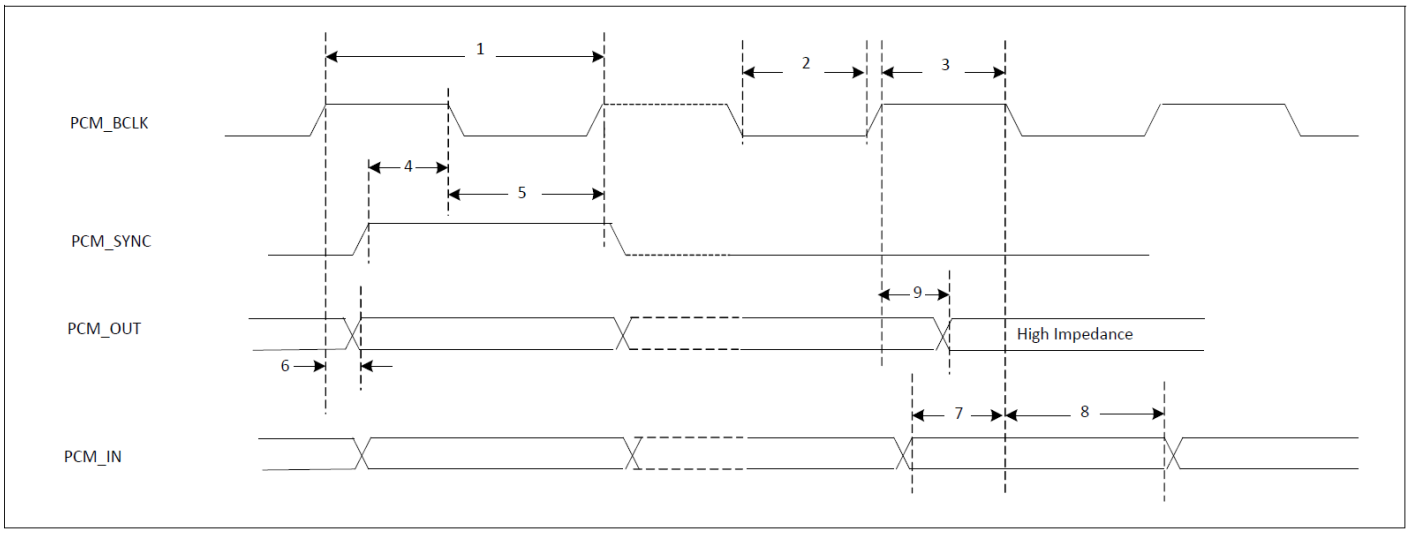

PCM Timing Diagram(Short Frame Sync, Slave Mode)

	Reference Characteristics	Minimum	Typical	Maximum	Unit
1	PCM bit clock frequency			12	MHz
2	PCM bit clock low	41			ns
3	PCM bit clock high	41			ns
4	PCM_SYNC setup	8			ns
5	PCM_SYNC hold	8			ns
6	PCM_OUT delay	0		25	ns
7	PCM_IN setup	8			ns
8	PCM_IN hold	8			ns
9	Delay from rising edge of PCM_BCLK during last bit period to PCM_OUT becoming high impedance	0		25	ns

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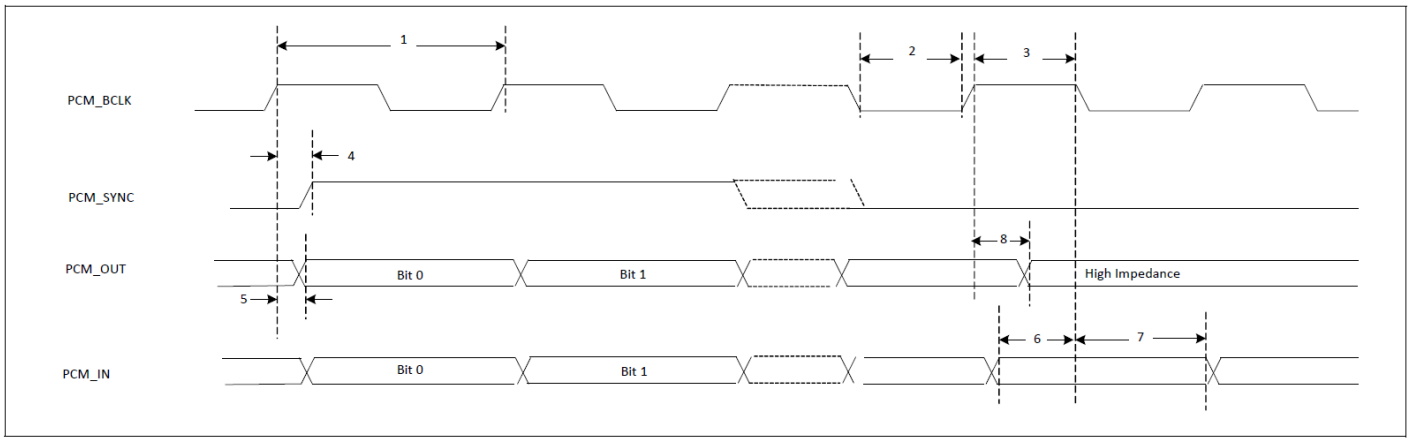
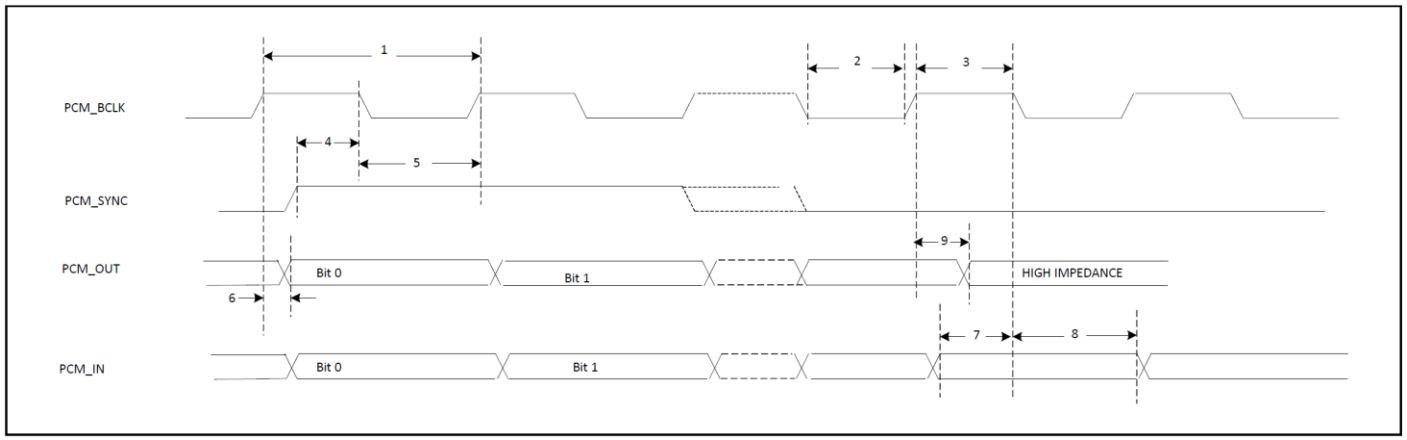


PCM Timing Diagram(Long Frame Sync, Master Mode)

	Reference Characteristics	Minimum	Typical	Maximum	Unit
1	PCM bit clock frequency			12	MHz
2	PCM bit clock low	41			ns
3	PCM bit clock high	41			ns
4	PCM_SYNC delay	0		25	ns
5	PCM_OUT delay	0		25	ns
6	PCM_IN setup	8			ns
7	PCM_IN hold	8			ns
8	Delay from rising edge of PCM_BCLK during last bit period to PCM_OUT becoming high impedance	0		25	ns



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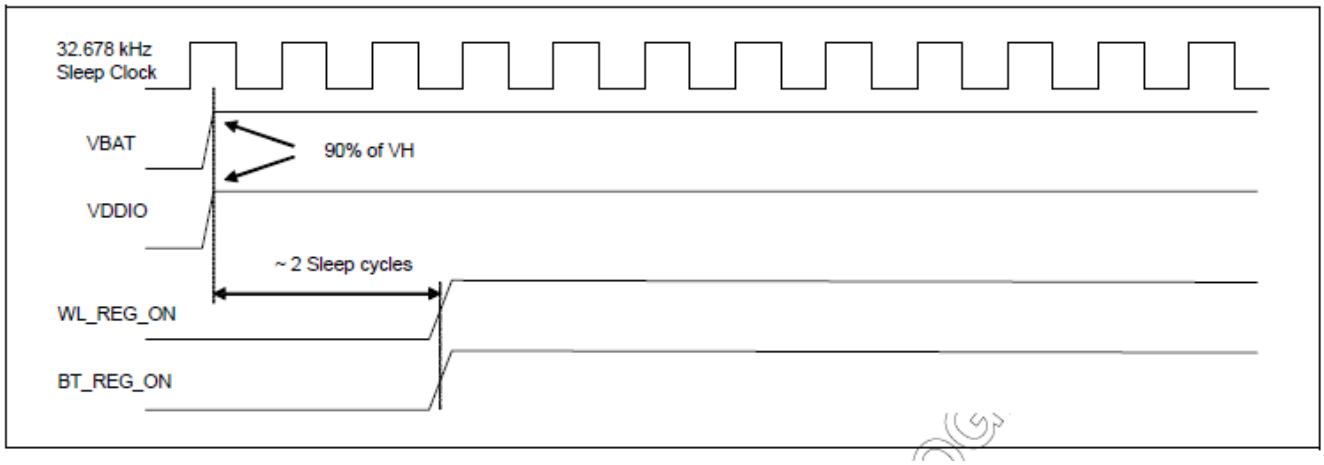
PCM Timing Diagram(Long Frame Sync, Slave Mode)

	Reference Characteristics	Minimum	Typical	Maximum	Unit
1	PCM bit clock frequency			12	MHz
2	PCM bit clock low	41			ns
3	PCM bit clock high	41			ns
4	PCM_SYNC setup	8			ns
5	PCM_SYNC hold	8			ns
6	PCM_OUT delay	0		25	ns
7	PCM_IN setup	8			ns
8	PCM_IN hold	8			ns
9	Delay from rising edge of PCM_BCLK during last bit period to PCM_OUT becoming high impedance	0		25	ns

3.5 Power up Timing Sequence

WLAN = ON, Bluetooth = ON



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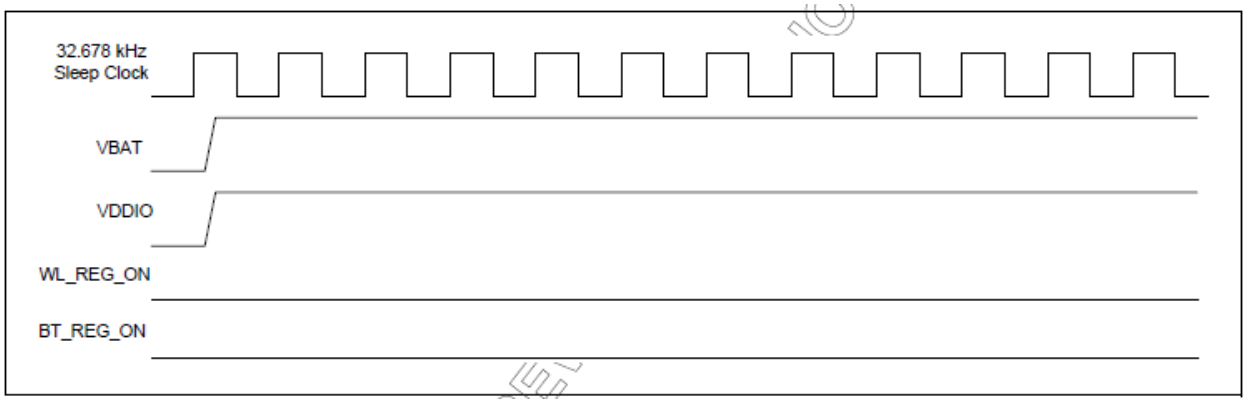
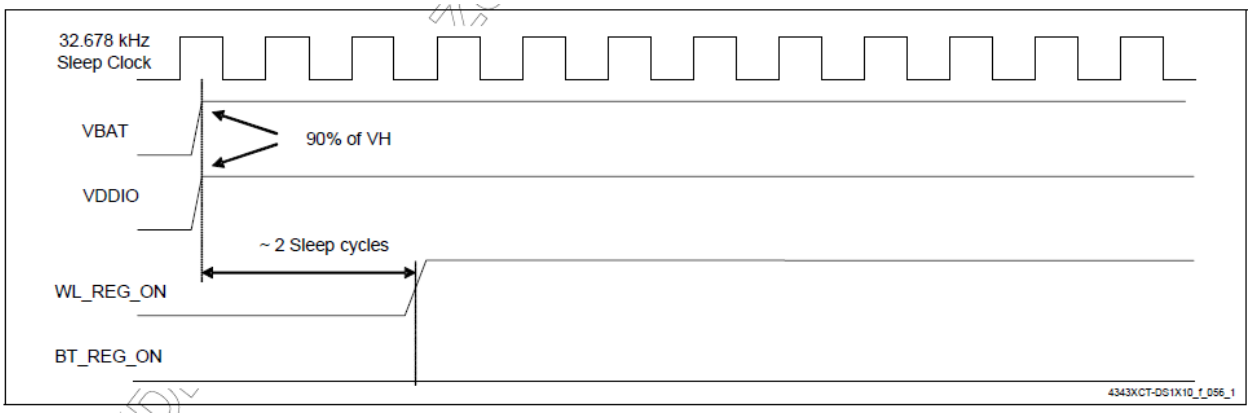
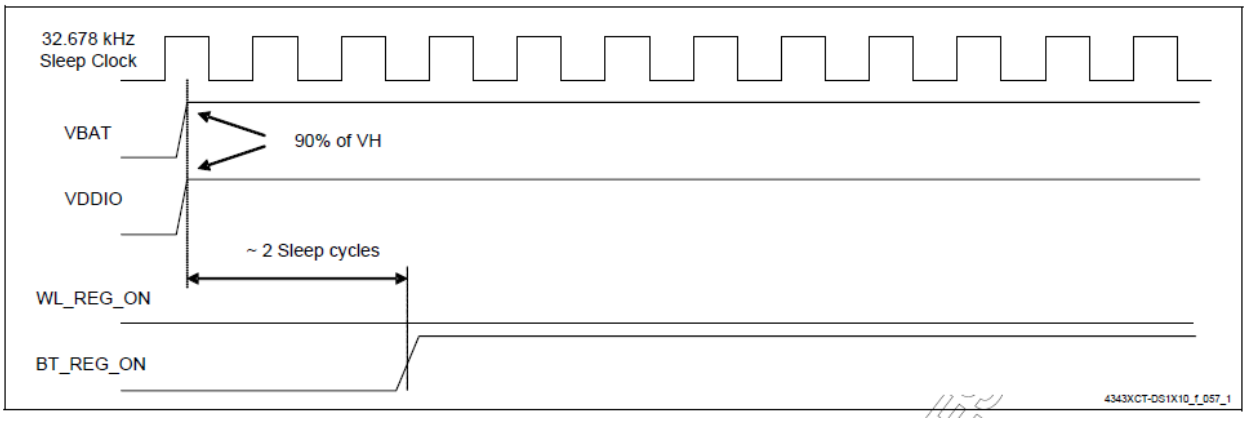
WLAN = OFF, Bluetooth = OFF



WLAN = ON, Bluetooth = OFF



WLAN = OFF, Bluetooth = ON



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3.6 Frequency References

The AW-NM512 uses an external 26MHz xtal for normal operation and an external secondary low frequency clock for low-power-mode timing. Either the internal low-precision LPO or an external 32.768 kHz precision oscillator is required. The internal LPO frequency range is approximately 33 kHz ± 30% over process, voltage, and temperature, which is adequate for some applications. However, a trade-off caused by this wide LPO tolerance is a small current consumption increase during WLAN power save mode that is incurred by the need to wake up earlier to avoid missing beacons.

The preferred approach for WLAN is to connect a precision external 26MHz & 32.768 kHz clock that meets the requirements listed in Table below.

Parameter	Conditions/Notes	Crystal			External Frequency Reference			
		Min.	Typ.	Max.	Min.	Typ.	Max.	Units
Frequency			26			26		MHz
Crystal load capacitance			12					pF
ESR				60				Ohms
Drive level	External crystal must be able to tolerate this drive level	200						uW
Input Impedance (XTAL_IN)	Resistive				10k	100k		Ohms
	Capacitive						7	pF
Input Voltage(XTAL_IN)	AC-coupled analog signal				400		1260	mV(p-p)
Input Low Level(XTAL_IN)	DC-coupled digital signal				0		0.2	V
Input High Level(XTAL_IN)	DC-coupled digital signal				1		1.26	V
Frequency tolerance Initial + over temperature		-20	0	20	-20	0	20	ppm

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Parameter	LPO	Units
Nominal input frequency	32.768	kHz
Frequency accuracy	+-200	ppm
Duty cycle	30 - 70	%
Input signal amplitude	200 - 3300	mV , p-p
Input impedance	>100	kΩ
	<5	pF
Signal type	Square-wave or sine-wave	-
Clock jitter (during initial start-up)	<10000	ppm

3.7 Power Consumption*

3.7.1 WLAN

Band (GHz)	Mode	BW (MHz)	RF Power (dBm)	Transmit			Receive	
				Max.	Avg.	Duty. (%)	Max.	Avg.
2.4 (5)(6)	11b@1Mbps	20	17	TBD	TBD	TBD	TBD	TBD
	11b@11Mbps	20	17	TBD	TBD	TBD	TBD	TBD
	11g@6Mbps	20	15	TBD	TBD	TBD	TBD	TBD
	11g@54Mbps	20	15	TBD	TBD	TBD	TBD	TBD
	11n@MCS0	20	13	TBD	TBD	TBD	TBD	TBD
	11n@MCS7	20	13	TBD	TBD	TBD	TBD	TBD

Current Unit: mA
(5)Using MFG firmware.
(6)Using LeCroy to measuare Duty cycle's Max and recoard Measure->Mean , Mean= Avg

3.7.2 Bluetooth

No.	Mode	Packet Type	VBAT_IN=3.3 V	
			Max.	Avg.
1.	Deepsleep	N/A	TBD	TBD
2.	Transmit	DH5	TBD	TBD
3.	Receive	3-DH5	TBD	TBD

* The power consumption is based on Azurewave test environment, these data for reference only.

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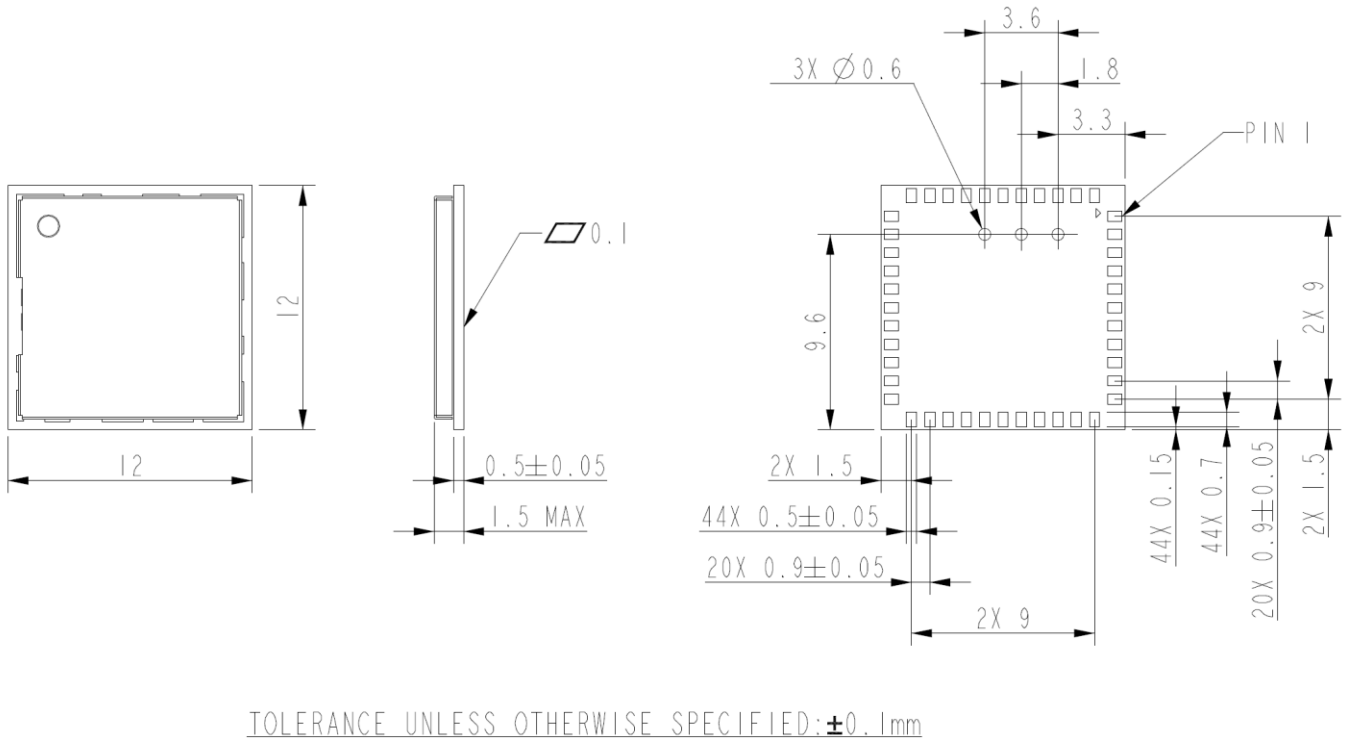
4. Mechanical Information

4.1 Mechanical Drawing



TOLERANCE UNLESS OTHERWISE SPECIFIED:±0.1mm

Unit:mm

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5. Packaging Information

5.1

5.2

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5.3

PINK BUBBLE WRAP

5.4

AFFIX PACKING LABEL

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5.5

1.5K/reel, 7.5K / carton

5.6

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